Volume 07 Issue 02 Published, May 21, 2003 ISSN 1535-864X

Intel® Technology Journal

Intel® Centrino™ Mobile Technology

Innovation Brings Low Power Integrated Graphics to the Intel® Centrino™ Mobile Technology Platform

Innovation Brings Low Power Integrated Graphics to the Intel® Centrino™ Mobile Technology Platform

Shailesh Trivedi, Mobile Chipsets & Graphics Engineering, Intel Corporation
Tom Shewchuk, Mobile Chipsets & Graphics Engineering, Intel Corporation
Aditya Sreenivas, Mobile Chipsets & Graphics Engineering, Intel Corporation
Terry Fletcher, Design Automation & Technology Engineering, Intel Corporation
Michael de la Cruz, Mobile Product Marketing, Intel Corporation

Index words: 855GM, Pentium® M, Validation, Centrino

ABSTRACT

The Intel® 855GM chipset brings breakthrough integrated graphics performance and low power to Intel® Centrino™ mobile technology platforms. To support the mobility vectors of battery life and performance, several power/performance features were designed into the chipset microarchitecture. Aggressive Clock Gating reduces the average power of the integrated graphics engine. Delay Locked Loop (DLL) Power Down reduces power by managing the system memory bandwidth of the Unified Memory Architecture (UMA). DRAM row power management reduces Dual In-line Memory Module (DIMM) system power. These innovative features push the cutting edge of the power/performance envelope establishing Intel Centrino as the best solution for mobile platforms. This paper describes these microarchitecture-level features, the process used to validate them, and the power measurement results from silicon. An overview of the future challenges is also presented.

INTRODUCTION

Intel Centrino mobile technology is based on the understanding that mobile customers value the four vectors of mobility: performance, battery life, small form factor, and wireless connectivity (see Figure 1). The performance and battery life vectors pose unique challenges, as improvements in performance generally reduce battery life. Key innovation is required to increase performance significantly from one product generation to the next, while at the same time enabling extended battery life to approach the end goal of more than eight hours of usage with a single battery. This paper summarizes key microarchitectural features that were designed into the Intel 855GM chipset with integrated graphics. These features cover the graphics engine, main memory power management features such as dynamic row power down and Graphics Memory Controller Hub (GMCH) Dynamic Input/Output Delay Locked Loop (IO/DLL) Power Management. The key lesson learned during this development effort is that the best mobile chipsets are optimized specifically for both performance and low power from the architectural definition through the validation effort, ultimately resulting in excellent silicon results.

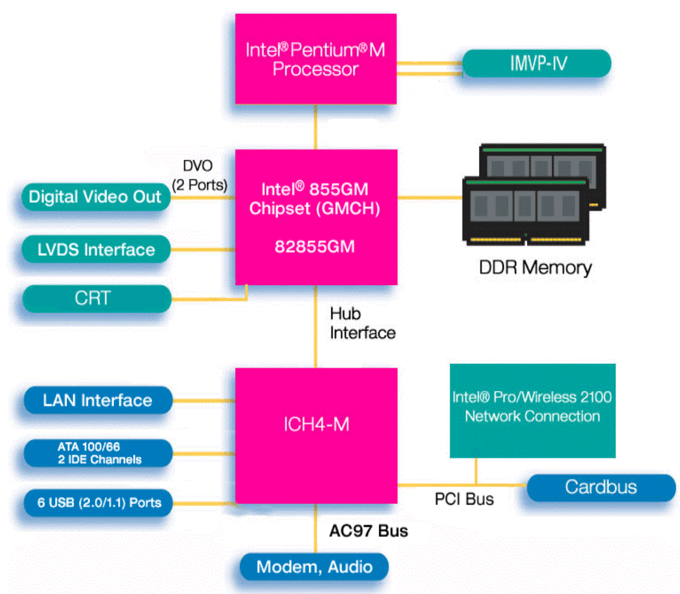

Figure 1: Intel® Centrino™ mobile technology platform

POWER MANAGEMENT FEATURES

Main Memory Power Management

The main memory is power managed during normal operation and in low-power Advanced Configuration and Power Interface (ACPI) Cx states. Each row has a separate CKE (clock enable) pin that is used for power management.

Dynamic Row Power Down is employed during normal operation. Based on idle conditions in a given row of memory, that memory row may be powered down. If the pages for a row have all been closed at the time of power down, then the device will enter the active power down state. If pages remain open at the time of power down the devices will enter the precharge power down state.

GMCH Dynamic IO/DLL Power Management

The Graphics Memory Controller Hub (GMCH) employs several mechanisms to reduce die power due to IO traffic: Memory Address and command signal tri-state are used when all memory is in power down or self-refresh. Memory Chip-select tri-state is used for a powered-down row. Memory Clock tri-state is used when memory is in self-refresh. Memory Clock tri-state is used for unpopulated Dual In-line Memeory Modules (DIMMs). Memory CKE/CS tri-state is used for unpopulated rows. Memory input buffer sense amps are disabled when no data are pending. Processor Bus Dynamic On Die Termination (ODT) is disabled when GMCH is driving. Address and control sense amps are disabled in C2 states and below unless GMCH is performing a snoop. Address and control sense amps are disabled when the BREQ0# pin is not asserted by the CPU. Data bus sense amps are disabled unless the GMCH is receiving data from the CPU. All sense amps are disabled in C3 and below. Special consideration is applied to memory IO control Delay Locked Loops (DLLs) because of the power they consume.

DLLs are used in the system memory interface to adjust input timings for the data strobe (DQS) signals as well as to fine tune the timing of the RCVEN signal. Each full DLL design includes two parts: a master and a slave. Both master and slave are separate delay lines with adjustable delay elements. The master calibrates the delay elements to tune its entire delay line to match the duration of a reference clock. The slave uses the calibration information determined by the master to adjust the delay for its own delay elements. The slave is the actual delay line that is used to delay a functional signal (i.e., DQS input) and can be selected to use a variable number of its calibrated delay elements to form a specific stable delay for this functional signal. Because of the different behaviors of the master and slave, there is a difference in the amount of time it takes to re-enable each after having powered them down, which is why they may be treated separately as explained below.

To reduce power consumption wherever possible, the SM DLLs are disabled when possible. This behavior is configurable, but the target behavior is shown in the table below. In addition to this the DLLs are disabled during leakage test mode (IDDQ).

Table 1: Targeted DLL state conditions

CPU/System State	DLL States with Internal Graphics
C0, C1, C2	Masters and Slaves enabled
C3, C4	If the graphics engine is idle, there are no display requests, and display configuration is permitted, then disable DLL
S3-Hot	Disable DLL
S4, S5	Power Off

Validation Methodology

Pre-silicon power management validation required the development of capabilities on multiple fronts.

- Model all system-level hardware components for logic simulation.
- Conduct formal reviews of circuit-level components that were difficult to model.
- Test methodology at the full system and sub-system levels.
- Emulate hardware.
- Validate the BIOS in a pre-silicon environment.

We will review each area in detail.

Modeling Components For Logic Simulations

Power management functionality is based on complex interactions between the CPU, the GMCH, the IO Controller Hub (ICH), the system Clock Generator (CG) chip and the Voltage Regulator (VR). To ensure that all the power management transactions and handshakes function as designed, each of these components has to be modeled at a level of detail that allows the transactions to be verified. The GMCH and the ICH bear the bulk of the burden of functionality of all the power management transactions. For full-system modeling, we used the detailed RTL models for the GMCH and the ICH. It was critical to ensure that circuit-level sub-units such as Phase

Lock Loops (PLLs) and DLLs needed to be modeled correctly to ensure that the enabling and disabling of these blocks functioned correctly during the various power management states. The CPU, CG, and VR models were behavioral models that were pin accurate for transaction signaling.

Reviewing Circuit-Level Components

In certain power-management states, the power to the logic core is turned off and the DRAM memory enters a low-power state. At this time, there is minimal leakage current consumed by the CPU, GMCH, and ICH. The IO buffers connected to the DRAM in the GMCH need to remain powered on to keep the memory alive. This requires careful design to ensure that a valid wakeup event brings up the system without any glitches or memory corruption. Due to the analog nature of the IO buffer circuits, they are inherently difficult to model and simulate using a system-level logic simulator. The only robust method to ensure that these power-down and power-up sequences work correctly is through thorough design reviews with circuit and system designers who understand the IO buffer circuits and the power-management events that are expected to occur. Such due diligence reviews require inter-disciplinary participation from analog circuit designers and power-management architects.

Testing Methodology

Once the components are modeled correctly, the quality of the design depends on the quality of the test plans and tests that are written. Testing was accomplished at four distinct levels with different test methodologies.

Unit Level: Each unit within the GMCH that was responsible for any power management functionality was tested using hand-crafted tests that validated specific features and functionality.

Super-Unit Level: A super-unit is a group of related units that interact with each other to form a sub-system. The chipset super unit was responsible for all the CPU, DRAM, and ICH traffic cycles. The super unit was modeled in RTL code; the external components were all modeled with behavioral code. The tests written at this level included a small set of hand-crafted power-management tests and a large set of complex random tests used to stress the power management functionality across all the aforementioned interfaces of the GMCH.

Full System Level: The full system models are the CPU, CG, and VR with behavioral models as mentioned earlier. The GMCH and ICH are modeled at the detailed RTL level. The test generation at this level was primarily done using random test generation tools, which had a finer control of the GMCH and ICH, since they are modeled at the RTL level.

Hardware Emulation

The final piece to the pre-silicon validation environment was the hardware emulation environment. This comprised a Quickturn emulator that emulated the detailed RTL models of the GMCH and ICH. The CPU in this case was a real chip, and the clock generator was an FPGA-based model. This environment gave us more than 100X speedup over the software simulation environment and enabled us to run several thousand cycle combinations of various power-management events. This environment was also a key capability that enabled us to get the mobile BIOS code validated before silicon.

BIOS Validation

BIOS plays a key role in ensuring that the chipsets enter and exit correctly from the various ACPI power-management states. This is the central software piece that ties the system components together, programs the appropriate configuration registers, and handles the state transition events via special blocks of code called handlers. In order to truly validate the BIOS, real silicon and a real system are required. Hence pre-silicon validation of the BIOS is a real challenge. In the case of the 855GM chipset, the power management code base of the BIOS was validated on an 845G platform. This enabled us to validate the BIOS code pertaining to all the “desktop” ACPI states. The “mobile” code base of the BIOS required us to validate the BIOS on a hardware emulator. The overall effort ensured that our BIOS were healthy on first silicon, and we were testing power-management cycles before the end of the first week after receiving prototype samples of the GMCH.

SILICON RESULTS

As low power was a major focus area of the Intel 855GM chipset, it was important to track the power level at all phases during product development. During the product definition phase, targets for peak and average power were established based on the levels achieved on current and past Intel integrated graphics chipsets. The targets were set with the goal of achieving lower power than previous chipset products while increasing performance. The results are shown at the end of this section.

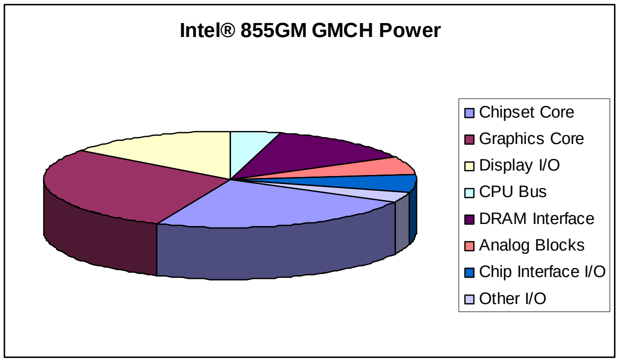

Figure 2: Intel® 855GM power breakdown

During both pre- and post-silicon phases, the power was tracked with a spreadsheet as a sum of individual components, shown in Figure 2. Design features and properties were updated in the spreadsheet model during the design phase, which helped in several ways:

- Power could be tracked against targets as parameters changed.
- Items with the largest power contribution could receive the most focus.
- Power-saving features could be compared to the baseline for Return on Investment feasibility studies.

As with most programs, increased performance requirements during the planning phase pushed the power projection higher. By using the tracking spreadsheet, there was a closed loop process to ensure that the designers were aware of how far they exceeded the target with new design innovations. Figure 3 shows that without the lower power design, the Intel 855GM chipset's power would have potentially been 1.1W higher for peak, and 0.7W higher for average.

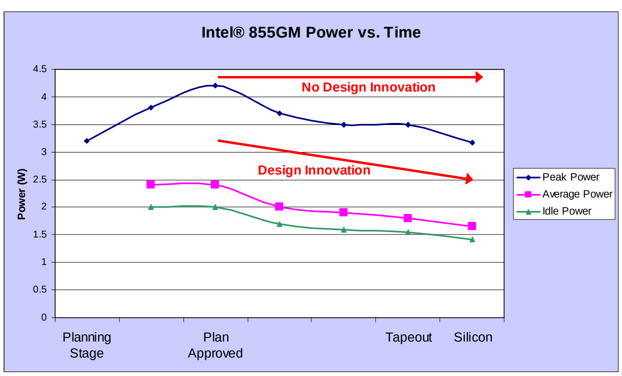

Figure 3: Intel® 855GM power vs. design phase

One design technique incorporated into the GMCH to reduce GMCH power consumption is Aggressive Clock Gating. Clock Gating is not a new technique, but it must be specifically architected for an integrated graphics controller and implemented intelligently to be effective. In the Intel 855GM chipset, clock gating is controlled at both the unit level and the partition level. In theory, this not only yields a power savings when not performing any work (the general idea behind clock gating), but it also takes advantage of the mutual exclusivity of the partitions under a heavy workload. The results in Figure 4 show significant power savings at idle, as well as savings under a sample intense graphics workload. The example shows three partitions (2D, 3D, and Memory Interface) with their individual clock gating disabled to show the impact to core power. By aggressively targeting mutually exclusive units in each partition, a savings is realized even under an intense workload.

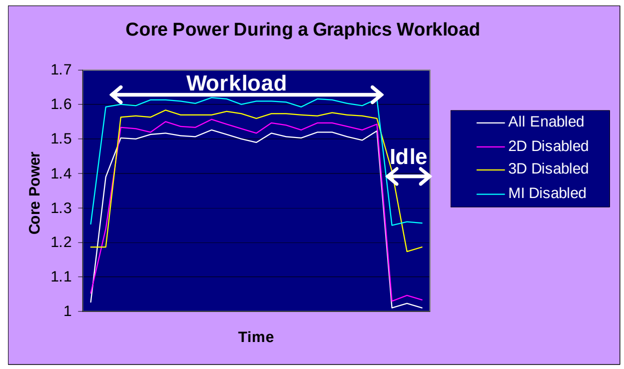

Figure 4: Clock gating impact to core power

Ultimately, the Intel 855GM program and performance goals were achieved; Intel 855GM graphics performance is almost double the performance of the previous generation Intel 830M integrated graphics chipset while keeping the amount of power consumed at or below levels attained on the Intel 830M.

FUTURE CHALLENGES

Even though excellent performance and power results were achieved on Intel Centrino mobile technology systems that contain the Intel 855GM chipset, there is no time to rest. New features are coming to mobile platforms including dual-channel Double Data Rate (DDR), larger LCD panels, and higher graphic demands with Microsoft's new 3D user interface. All these platform enhancements will make tomorrow's mobile platforms exciting. However, the mobile customer will not accept these features if battery life is compromised. Thus the challenge for next-generation Intel Centrino mobile technology is to bring these new feature enhancements to market while enabling longer battery life. This challenge can be broken down into three areas. The first is obviously to control chipset average power consumption, ensuring that the Intel components of future Intel Centrino systems minimize average power consumption as much as

possible. The second is to focus on reducing power consumed by the highest power hogs in today's mobile platforms, namely system memory Dual In-line Memeory Modules (DIMMs) and the LCD panel. The final area that cannot be ignored is the need to reduce the power of all remaining platform components.

CONCLUSION

Intel Centrino mobile technology delivers on all four vectors of mobility. The Intel 855GM chipset delivers breakthrough integrated graphics performance and enables extended battery life. Aggressive Clock Gating allows the graphics engine to significantly increase performance while controlling average power. DLL Power Down enables system memory bandwidth to double for single data rate-based systems, while reducing average power consumption. DRAM row power management reduces overall DIMM system power, thus driving the entire platform power down. All of these innovations were achieved by executing a chipset development effort focused primarily on optimizing breakthrough integrated graphics performance at lower power. With the tremendous excitement generated by the introduction of Intel Centrino mobile technology, it is clear that the mobile customer will continue to demand continuous innovation in future notebook systems. Intel Centrino mobile technology will continue to deliver the needed innovation to advance performance, battery life, form factor, and wireless connectivity.

AUTHORS' BIOGRAPHIES

Shailesh Trivedi is the validation manager for Mobile Chipset and Graphics Component Engineering. During the past 17 years he has worked on automotive controllers, microprocessors, and chipsets. He has an M.S.E.E. degree from the University of Michigan at Ann Arbor and has been with Intel since 1991. His e-mail is shailesh.b.trivedi@intel.com.

Tom Shewchuk was the Intel 855 chipset program manager, and currently is managing Intel's next-generation mobile chipsets. He has B.S.E.E., M.S.EE, and M.B.A. degrees, all from the University of Illinois at Urbana-Champaign. After jobs at Honeywell and Ford Microelectronics, he joined Intel in 1991, spending his first five years working on microprocessors, and the past seven years working on integrated graphics chipsets. His e-mail is tom.j.shewchuk@intel.com.

Aditya Sreenivas was the lead microarchitect for the Intel 855GM chipset, and is the lead microarchitect for Mobile Chipset and Graphics Component Engineering. He has an M.S.degree in Electrical Engineering from Arizona State University. He joined Intel in 1991 working in the chipset division and has worked on a variety of desktop and mobile chipsets. His e-mail is aditya.sreenivas@intel.com.

Terry Fletcher was the owner of the Power-Thermal Working Group for the Intel 855GM chipset, and is the lead power engineer for desktop and mobile chipsets. He has a B.S. degree in Engineering and Physics from the University of the Pacific. He joined Intel as a co-op in 1997 in the Chipset Division, and he began full-time as a power engineer the following year, where he continues to analyze and address the ever-increasing importance of power in graphics and chipsets. His e-mail is terry.fletcher@intel.com.

Michael de la Cruz is the Intel 855 chipset product marketing manager. He has a B.S.E.E. degree from Carnegie Mellon University and an M.B.A. degree from Johnson Graduate School of Management at Cornell University. After working at PictureTel Corporation, he joined Intel in 1999, working on wireless initiatives and chipset products for Intel Mobile Products Group. His e-mail is michael.de.la.cruz@intel.com

For further information visit:

developer.intel.com/technology/itj/index.htm